CLAIMS

What is claimed is:

1. A register file for a data processing system comprising:

a memory unit having a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register and processor mode;

input ports to receive inputs for addressing at least one of the memory locations using an encoded address; and

output ports to output data from at least one of the memory locations addressable by an encoded address.

2. The register file of claim 1, wherein a plurality of registers correspond to the plurality of memory locations of the memory unit.

3. The register file of claim 2, wherein each register is addressable by a corresponding encoded address.

4. The register file of claim 3, wherein at least two registers are capable of being accessed in different processor modes using the same encoded address.

5. The register file of claim 1, wherein the plurality of memory locations are discontinuous in the memory unit.

6. The register file of claim 1, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

7. The register file of claim 2, wherein inputs are received associated with at least one register and processor mode, and wherein at least one of the outputs is data from a register associated with an encoded address obtained from the received inputs.

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HENDERSON
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DUNNER LLP

1300 I Street, NW
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202.408.4000
Fax 202.408.4400
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8. The register file of claim 7, wherein data is outputted from the memory unit for at least two instructions.

9. The register file of claim 2, wherein inputs are associated with at least one register and processor mode, and wherein one of the inputs is data to be written in a register associated with an encoded address obtained from the received inputs.

10. The register file of claim 9, wherein data for at least two retired instructions is to be written in at least two registers.

11. The register file of claim 1, further comprising:

an address encoder for each input port, the address encoder to provide an encoded address for accessing one of the memory locations.

12. The register file of claim 11, further comprising:

a latch to latch an encoded address from the address encoder; and

a selector coupled to the latch and the address encoder, the selector to select the encoded address from either the latch or the address encoder.

13. The register file of claim 10, wherein the latch stores the encoded address as a pipeline storage of the encoded address.

14. A register file for a data processing system comprising:

memory means having a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register means and processor mode;

input means to receive inputs for addressing at least one of the memory locations using an encoded address; and

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output means to output data from at least one of the memory locations addressable by an encoded address.

15. The register file of claim 14, wherein a plurality of register means correspond to the plurality of memory locations of the memory means.

16. The register file of claim 15, wherein each register means is addressable by a corresponding encoded address.

17. The register file of claim 16, wherein at least two register means are capable of being accessed in different processor modes using the same encoded address.

18. The register file of claim 14, wherein the plurality of memory locations are discontinuous in the memory means.

19. The register file of claim 14, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

20. The register file of claim 16, wherein inputs are received associated with at least one register means and processor mode, and wherein at least one of the outputs is data from a register means associated with an encoded address obtained from the received inputs.

21. The register file of claim 20, wherein data is outputted from the memory means for at least two instructions.

22. The register file of claim 15, wherein inputs are associated with at least one register means and processor mode, and wherein one of the inputs is data to be written in a register means associated with an encoded address obtained from the received inputs.

23. The register file of claim 22, wherein data for at least two retired instructions is to be written in at least two register means.

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24. The register file of claim 14, further comprising:

addressing means for each input port, the addressing means to provide an encoded address for accessing one of the memory locations.

25. The register file of claim 24, further comprising:

latching means to latch an encoded address from the address encoder; and

selecting means coupled to the latching means and the addressing means, the selecting means to select the encoded address from either the latching means or the addressing means.

26. The register file of claim 23, wherein the latching means stores the encoded address as a pipeline storage of the encoded address.

27. A data processing system comprising:

a processor to process instructions including:

a plurality of pipeline stages to execute instructions including a register file, the register file including

a memory unit having a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register and processing mode;

input ports to receive inputs for addressing at least one of the memory locations using an encoded address; and

output ports to output data from at least one of the memory locations using an encoded address.

28. The data processing system of claim 27, wherein a plurality of registers correspond to the plurality of memory locations of the memory unit.

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29. The data processing system of claim 28, wherein each register is addressable by a corresponding encoded address.

30. The data processing system of claim 29, wherein at least two registers are capable of being accessed in different processor modes using the same encoded address.

31. The data processing system of claim 27, wherein the plurality of memory locations are discontinuous in the memory unit.

32. The data processing system of claim 27, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

33. The data processing system of claim 28, wherein inputs are received by the memory unit associated with at least one register and processor mode, and wherein at least one of the outputs from the memory unit is data from a register associated with an encoded address obtained from the received inputs.

34. The data processing system of claim 33, wherein data is outputted from the memory unit for at least two instructions.

35. The data processing system of claim 28, wherein inputs to the memory unit are associated with at least one register and processor mode, and wherein one of the inputs to the memory unit is data to be written in a register associated with an encoded address obtained from the received inputs.

36. The data processing system of claim 35, wherein data for at least two retired instructions is to be written in at least two registers.

37. The data processing system of claim 27, wherein the pipeline stages include:

an instruction fetch stage to fetch one or more instructions; and

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1300 I Street, NW
Washington, DC 20005
202.408.4000
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an instruction decode stage to decode fetched instructions from the instruction fetch stage, the instruction decode stage to forward inputs to the input ports of the memory unit of the register file for outputting data from or writing data to one or more of the memory locations;

an execution stage including a plurality of execution units, each execution unit to receive data from the memory unit for executing an instruction; and

a write back or retire logic stage to receive results data associated with one or more instructions executed by the execution units of the execution stage, and to forward the results data to the memory unit of the register file for storage.

38. The data processing system of claim 27, wherein the processor is at least one of an embedded processor or a microprocessor.

39. A data processing system comprising:

processing means for processing instructions including:

pipeline means for executing instructions including a register file means, the register file means including

memory means having a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register means and processing mode;

input means to receive inputs for addressing at least one of the memory locations using an encoded address; and

output means to output data from at least one of the memory locations using an encoded address.

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40. The data processing system of claim 39, wherein a plurality of register means correspond to the plurality of memory locations of the memory means.

41. The data processing system of claim 40, wherein each register means is addressable by a corresponding encoded address.

42. The data processing system of claim 41, wherein at least two register means are capable of being accessed in different processor modes using the same encoded address.

43. The data processing system of claim 39, wherein the plurality of memory locations are discontinuous in the memory means.

44. The data processing system of claim 39, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

45. The data processing system of claim 39, wherein inputs are received by the memory means associated with at least one register means and processor mode, and wherein at least one of the outputs from the memory means is data from a register means associated with an encoded address obtained from the received inputs.

46. The data processing system of claim 45 wherein data is outputted from the memory means for at least two instructions.

47. The data processing system of claim 40, wherein inputs to the memory means are associated with at least one register means and processor mode, and wherein one of the inputs to the memory means is data to be written in a register means associated with an encoded address obtained from the received inputs.

48. The data processing system of claim 47, wherein data for at least two retired instructions is to be written in at least two register means.

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49. The data processing system of claim 39, wherein the pipeline means further includes:

instruction fetching means to fetch one or more instructions; and

instruction decoding means to decode fetched instructions from the instruction fetching means, the instruction decoding means to forward inputs to the input ports of the memory means of the register file means for outputting data from or writing data to one or more of the memory locations;

execution means including a plurality of functional means, each functional means to receive data from the memory unit for executing an instruction; and

logic means to receive results data associated with one or more instructions executed by the functional means of the execution means, and to forward the results data to the memory means of the register file means for storage.

50. The data processing system of claim 39, wherein the processing means is at least one of an embedded processing means and a microprocessing means.

51. A processor comprising:

an integrated circuit including

a memory unit having a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register and processor mode; and

at least one address encoder to provide at least one encoded address for addressing at least one of the memory locations.

52. The processor of claim 51, wherein a plurality of registers correspond to the plurality of memory locations in the memory unit.

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53. The processor of claim 52, wherein each register is addressable by a corresponding encoded address.

54. The processor of claim 53, wherein at least two registers are capable of being accessed in different processor modes using the same encoded address.

55. The processor of claim 51, wherein the plurality of memory locations are discontinuous in the memory unit.

56. The processor of claim 51, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

57. The processor of claim 51, wherein each address encoder includes input ports to receive inputs associated with at least one register and processor mode in providing a corresponding encoded address.

58. The processor of claim 57, wherein each address encoder includes logic circuitry to obtain the corresponding encoded address based on the received inputs.

59. The processor of claim 58, wherein the logic circuitry includes at least one of a programmable gate array (PGA) or a field programmable gate array (FPGA).

60. The processor of claim 51, wherein the processor is at least one of an embedded processor and a microprocessor.

61. A data processing system comprising a memory mapped register file for accessing a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register and processor mode.

62. The data processing system of claim 61, wherein a plurality of registers correspond to the plurality of memory locations.

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63. The data processing system of claim 62, wherein each register is addressable by a corresponding encoded address.

64. A processor comprising:

circuit means including

memory means having a plurality of memory locations, each memory location being addressable by an encoded address, wherein the encoded address corresponds to at least one register means and processor mode; and

at least one addressing means to provide at least one encoded address for addressing at least one of the memory locations.

65. The processor of claim 64, wherein a plurality of register means correspond to the plurality of memory locations of the memory unit.

66. The processor of claim 65, wherein each register means is addressable by a corresponding encoded address.

67. The processor of claim 66, wherein at least two register means are capable of being accessed in different processor modes using the same encoded address.

68. The processor of claim 64, wherein the plurality of memory locations are discontinuous in the memory means.

69. The processor of claim 64, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

70. The processor of claim 64, wherein each addressing means includes input means to receive inputs associated with at least one register means and processor mode in providing a corresponding encoded address.

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71. The processor of claim 70, wherein each addressing means includes logic means to obtain the corresponding encoded address based on the received inputs.

72. The processor of claim 71, wherein the logic means includes at least one of a programmable gate array (PGA) or a field programmable gate array (FPGA).

73. The processor of claim 64, wherein the processor is at least one of an embedded processor and a microprocessor.

74. An integrated circuit method comprising:

configuring the integrated circuit to receive inputs;

configuring the integrated circuit to determine an encoded address based on the received inputs, wherein the encoded address corresponds to at least one register and processor mode;

configuring the integrated circuit to access a register using an encoded address; and

configuring the integrated circuit to output data from the accessed register.

75. The method of claim 74, further comprising:

configuring the integrated circuit to output data for multiple instructions.

76. The method of claim 74, further comprising:

configuring the integrated circuit to write data to the accessed register.

77. The method of claim 76, further comprising:

configuring the integrated circuit to write data to one or more accessed registers for multiple executed instructions.

78. A method for accessing a memory unit having a plurality of memory locations comprising:

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receiving a memory request for accessing the memory unit, the memory request including a register index input and a processor mode input;

encoding the register index input and processor mode input to obtain an encoded address;

accessing at least one of the memory locations of the memory unit in accordance with the encoded address, wherein the encoded address corresponds to at least one register and processor mode; and

writing data into or reading data from the accessed memory location.

79. The method of claim 78, wherein writing data into or reading data from the accessed memory location includes writing data into or reading data from the accessed memory location for multiple instructions.

80. A memory unit comprising:

a plurality of memory locations addressable by encoded addresses, wherein each encoded address corresponds to at least one register and processor mode.

81. The memory unit of claim 80, wherein a plurality of registers correspond to the plurality of memory locations.

82. The memory unit of claim 81, wherein each register is associated with an index that maps to a corresponding encoded address based on at least one processor mode.

83. The memory unit of claim 82, wherein each encoded address is capable of mapping to one or more indices associated with a register and a particular processing mode.

84. The memory unit of claim 80, wherein the plurality of memory locations of the memory unit addressable by an encoded address are discontinuous.

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85. The memory unit of claim 80, wherein a bit width of the plurality of memory locations is scalable to any arbitrary bit width size.

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